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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,432	04/09/2004	Chen-Bau Wu	24061.148(TSMC2003-0893)	1237

42717 7590 02/13/2006

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ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,432	WU ET AL.	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *1,18 and 35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,13-26,30-41,45-53* is/are rejected.

7)☒ Claim(s) *10-12,27-29,42-44,53 and 54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendments to the specification are acknowledged and accepted. Amended claims are acknowledged and treated below. Claims 1, 18, 35 are cancelled and claims 52-54 have been added.

Response to Arguments

2. The independent claims rejected in the prior office action were amended to be more specific as to the inventions' metes and bounds. However prior art and new art still reads on most of these amended and dependent claims. The subsequent rejections herein may be repeated from the first office action dated 8/25/2005 for clarity.

Drawings

3. The drawings are objected to because the title for each of the three drawings has the phrase "TUNING-ON CHANNELS" whereas the phrase should read, "TU*R*NING-ON CHANNELS". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered

and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The examiner requires that the cross section figures 2-3 be resubmitted without shadings because the device structure in unclear. Per 37 CFR 1.84 under *sectional views* hatching must be used to indicate sectional views of an object.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim **53** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 53 reads "the semiconductor device of claim 52 wherein the deep trench is proximate to the first edge of the source and the first edge of the drain with a smaller distance relative to a dimension of the source perpendicular to the first edge of the source." The phrase, "a dimension of the source perpendicular to the first edge of the source",

could be taken to mean the width of the source between the first edge and the second edge of the source or it could mean a size of infinite or non-specific variable length since the word dimension can mean an orthogonal or perpendicular axis extending outward some unspecified amount. The examiner has assumed the first meaning is intended. The first meaning specifically being: in the applicant's Fig. 1 of the specification, the examiner interprets claim 53 to mean that the distance W_2 is less than distance W_1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **4,21,37** are rejected under 35 U.S.C. 102(b) as being anticipated by Joyner el al. (US Pat. 6,114,741).

Regarding claim **4**, Joyner teaches a semiconductor device [FIG. 2-3] comprising;

a substrate [FIG. 2, 10] including a source [S] and drain [D], the source [S] having a first edge [FIG. 3, horizontal line marked by 32] and the drain [D] having a first edge [same as the source] a gate [26] between the source [S] and drain [D], the gate [26] having a first portion [FIG. 3, horizontal line marked by 32]; and a first deep trench structure [FIG. 3; 22 adjacent to the horizontal line marked by 32] located directly under [See FIG. 2] the first portion of the gate viewed in a direction from the gate [26] to the substrate [10], and proximate to the first edge of the source [S] and the first edge of the drain [D], wherein the first deep trench structure [22] has a depth greater than to 0.5 um [column 3, lines 44-46, "The depth of the trench region may be virtually any depth to produce isolation between active region 12 and active region 14."].

Regarding claim **21,** Joyner teaches a semiconductor device [FIG. 2-3] comprising:

a substrate [10] including a source [S] and drain [D], the source having a first edge [as above] and the drain having a first edge [as above];

a gate electrode [26] on the substrate [10] and between the source [S] and drain [D], a first portion of the gate electrode [26] extending past the first edge [as above] of the source [S] and the first edge [as above] of the drain [D]; and

a first deep trench structure [22] located directly under the first portion [as above] of the gate electrode [26] viewed in a direction from the gate electrode [26] to the

substrate [10] and proximate to the first edge [as above] of the source [S] and the first edge [as above] of the drain [D], wherein the first deep trench structure [22] has a depth greater than 0.5 um [column 3, lines 44-46, "The depth of the trench region may be virtually any depth to produce isolation between active region 12 and active region 14."].

Regarding claim **37**, Joyner teaches a semiconductor device [FIG. 2-3] comprising:

a substrate [10] having a source [S] and drain [D], having widths that are substantially equal [see FIG. 3] and each having a first edge [as above] substantially located along a common line on the substrate [10];

a gate electrode [26] on the substrate [10] and between the source [S] and the drain [D], the gate electrode [26] having a first portion [as above] extending past the first edge [as above] of the source [S] and the first edge [as above] of the drain [D]; and

a first deep trench structure [22] located directly under the first portion [as above] of the gate electrode [26] viewed in a direction from the gate electrode [26] to the substrate [10], the first deep trench structure [22] parallel to the common line on the substrate [10] and proximate to the first edge [as above] of the source [S] and the first edge [as above] of the drain [D], wherein the first deep trench structure [26] is substantially deeper than 0.5 um [column 3, lines 44-46, "The depth of the trench region may be virtually any depth to produce isolation between active region 12 and active region 14."].

6. Claims **4,9,21,26,37,41** are rejected under 35 U.S.C. 102(e) as being anticipated by Hara et al (US Pat Pub 2004/0029355).

Regarding claim **4**, Hara teaches a semiconductor device [FIG. 4A-4B] comprising;

a substrate [1] including a source [13] and drain [13], the source [13] having a first edge [the horizontal line of FIG. 4B which extends from the lower edge of the source to the lower edge of the drain and passes under the gate electrode] and the drain [13] having a first edge [same as line as the source] a gate [11, 12] between the source [13] and drain [13], the gate [11, 12] having a first portion [the horizontal line of FIG. 4B which extends from the lower edge of the source to the lower edge of the drain and passes under the gate electrode]; and a first deep trench structure [7] located directly under [see FIG. 4B] the first portion [as above] of the gate [11, 12] viewed in a direction from the gate [11, 12] to the substrate [1], and proximate to the first edge [the horizontal line of FIG. 4B which extends from the lower edge of the source to the lower edge of the drain and passes under the gate electrode] of the source [13] and the first edge [the horizontal line of FIG. 4B which extends from the lower edge of the source to the lower edge of the drain and passes under the gate electrode] of the drain [13], wherein the first deep trench structure [7] has a depth greater than to 0.5 um [page 4, section 0066, "about 0.4um to 0.8um"].

Regarding claim **21,** Hara teaches a semiconductor device [FIG. 4A-4B] comprising:

a substrate [1] including a source [13] and drain [13], the source having a first edge [as above] and the drain [13] having a first edge [as above];

a gate electrode [12] on the substrate [1] and between the source [13] and drain [13], a first portion [as above] of the gate electrode [12] extending past the first edge [as above] of the source [13] and the first edge [as above] of the drain [13]; and

a first deep trench structure [7] located directly under [as above] the first portion [as above] of the gate electrode [12] viewed in a direction from the gate electrode [12] to the substrate [1] and proximate to the first edge [as above] of the source [13] and the first edge [as above] of the drain [13], wherein the first deep trench structure [7] has a depth greater than 0.5um [page 4, section 0066, "about 0.4um to 0.8um"].

Regarding claim **37**, Hara teaches a semiconductor device [FIG. 4A-4B] comprising:

a substrate [1] having a source [13] and drain [13], having widths that are substantially equal [see FIG. 4A-4B] and each having a first edge [as above] substantially located along a common line [the same line for s/d/gate] on the substrate [1];

a gate electrode [12] on the substrate [1] and between the source [13] and the drain [13], the gate electrode [12] having a first portion [as above] extending

past the first edge [as above] of the source [13] and the first edge [as above] of the drain [13]; and

a first deep trench structure [7] located directly under the first portion [as above] of the gate electrode [12] viewed in a direction from the gate electrode [12] to the substrate [1], the first deep trench structure [7] parallel to the common line on the substrate [as above] and proximate to the first edge [as above] of the source [13] and the first edge [as above] of the drain [13], wherein the first deep trench structure [7] is substantially deeper than 0.5 um [as above].

Regarding claims **9,26,41** Hara teaches the semiconductor device of claim 4 (or claims 21,37) wherein the device includes a strained MOS structure [Page 4, section 0065, 3].

7. Claims **50-53** are rejected under 35 U.S.C. 102(b) as being anticipated by Brand el al. (US Pat. 6,172,401).

Regarding claim **50,** Brand teaches a semiconductor device [Fig. 7-8] comprising:

a substrate [100] including a first well [Fig. 7, 120, p-well] of a first-type dopant [p] and a second well [Fig. 7, 135, n-well] of a second type dopants [n] the first well [120] being disposed laterally adjacent [see Fig. 7] the second well [135];

a source [Fig. 7, 155] formed in the first well [120] and drain [160] formed in the second well [135], the source [155] having a first edge [Fig. 8, horizontal

line connecting the lower horizontal edge of 155 to the lower horizontal edge of 165 passing under the gate 145] and the drain [160] having a first edge [same as source];

a gate electrode [145] on the substrate [100] and between the source [155] and drain [160], a first portion [Fig. 8, horizontal line connecting 155 to 165 passing under the gate 145] of the gate electrode [145] extending past the first edge [Fig. 8 shows the gate 145 extending past the edge of the active area 155 region and thus over the isolation region 110 being the horizontal line connecting to region 160] of the source [155] and the first edge [as above] of the drain [160];

a current channel located in a region where the gate electrode extends beyond the first edge of the source and the first edge of the drain, the current channel allowing a leakage current [the field oxide 110 acts as a very thick gate oxide thus lowering leakage in direct proportion the field oxide's thickness] to flow in the device; and

a first deep trench structure [110, column 4, lines 59-61] formed partially in the first well [120] and partially in the second well [135], located under the first portion [as above] of the gate electrode [145] and proximate to the first edge [as above] of the source [155] and the first edge of the drain [160], whereby the first deep trench structure [120] is located close enough to the first edge of the source [155] and the first edge of the drain [160] to substantially eliminate [field oxide's function] the leakage current flow through the current channel.

Brands structure is virtually identical to the applicant's drawings 1-3. Brand refers to 160 as a tap but is identical to the applicants "drain" [120].

Regarding claim **51,** Brand teaches a method of manufacturing a microelectronic device [Fig. 7-8], comprising:

forming [column 4 line 65 to column 5 line 15, Fig. 1-3] a substrate [100] including a first well [120] of a first-type dopant [p] and a second well [135] of a second type dopant [n] the first well [120] being disposed laterally adjacent the second well;

forming [column 5 line 59 to column 6 line 37,Fig. 5-6] a source [155] in the first well [120] and a drain [160] in the second well [135];

forming [column 5, lines 47-58, Fig. 4] a gate [145] between the source [155] and drain [160]; and

forming [column 4, lines 53-64, Fig. 1 & 8] a deep trench [110] structure partially in the first well [120] and partially in the second well [135], underlying a portion of the gate [145] and proximate to an edge of the source [155] and drain [160].

Regarding claim **52**, Brand teaches a semiconductor device [Fig. 7-8] comprising:

a substrate [100] including a first well [120] of a first type dopant [p] and a second well [135] of a second type dopant [n];

a source [155] disposed in the first well [120] and a drain [160] disposed in the second well [135], the source [155] having a first edge [as above] and the drain [160] having a first edge [as above];

a gate electrode [145] between the source [155] and drain [160]; and

a deep trench structure [155] located directly under [see Fig. 8] the gate electrode [145], and proximate to the first edge [as above] of the source [155] and the first edge [as above] of the drain [160].

Regarding claim **53**, Brand teaches the semiconductor device [Fig. 7-8] of claim 52 wherein the deep trench [110] is proximate to the first edge [as above] of the source [155] and the first edge [as above] of the drain [160] with a smaller distance relative to a dimension of the source [155] perpendicular to the first edge [as above] of the source [155]. Referring to the applicant's Fig. 1 of his specification, the examiner interprets this claim to mean that the distance W_2 is less than distance W_1. Brand teaches distance W_2 is equal to zero.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims **2-8,14-17,19-25,31-34,36-40,46-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. (US Pat. Pub. 2002/0038901) in further in view of Chen et al. (2003/0006476).

Regarding claim **4**, Kuroi teaches a semiconductor device [FIG. 1-2; 101] comprising;

a substrate [FIG. 4-5, 1] including a source [6] and drain [6], the source [6] having a first edge [FIG. 1, A2] and the drain [6] having a first edge [FIG. 1, A2] a gate [5] between the source and drain, the gate having a first portion [FIG. 1, the intersection of line A2 and element 5]; and

a first deep trench structure [FIG. 1, AR2; FIG. 2, 9] located directly under the first portion of the gate viewed in a direction from the gate to the substrate [see FIG. 1], and proximate to the first edge of the source [FIG. 1, line A2] and the first edge of the drain [FIG. 1, line A2], wherein the first deep trench structure [FIG. 1, AR2] has a depth equal to 0.5 um [Page 4, section 0069]. Kuroi does not teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claim **21**, Kuroi teaches a semiconductor device [FIG. 1-2; 101] comprising:

a substrate [FIG. 4-5, 1] including a source [6] and drain [6], the source having a first edge [FIG. 1, A2] and the drain having a first edge [FIG. 1, A2];

a gate electrode [5] on the substrate [1] and between the source [6] and drain [6], a first portion of the gate electrode [5] extending past the first edge [line A2] of the source [6] and the first edge [line A2] of the drain [6]; and

a first deep trench structure [AR2, 9; adjacent to line A2] located directly under the first portion [line A2] of the gate electrode [5] viewed in a direction from the gate electrode [5] to the substrate [1] and proximate to the first edge [line A2] of the source [6] and the first edge [line A2] of the drain [6], wherein the first deep trench structure [AR2] has a depth equal to 0.5 um [Page 4, section 0069]. Kuroi does not teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claim **37**, Kuroi teaches a semiconductor device [FIG. 1-2; 101] comprising:

a substrate [Fig. 4 and 5, 1] having a source [6] and drain [6], having widths that are substantially equal [see FIG. 1] and each having a first edge [Fig. 1, A2] substantially located along a common line [A1] on the substrate [1];

a gate electrode [Fig. 2; 5A, 5B] on the substrate [1] and between the source [6] and the drain [6], the gate electrode [5A, 5B] having a first portion [Fig.

1, the intersection of line A2 and element 5] extending past the first edge [A2] of the source [6] and the first edge [A2] of the drain [6]; and

a first deep trench structure [AR2, 9, adjacent to line A2] located directly under the first portion [Fig. 1, the intersection of line A2 and element 5] of the gate electrode [5A, 5B] viewed in a direction from the gate electrode [5A, 5B] to the substrate [1], the first deep trench structure [AR2] parallel to the common line [A1] on the substrate [1] and proximate to the first edge [A2] of the source [6] and the first edge [A2] of the drain [6], wherein the first deep trench structure [AR2] is equal to 0.5 um [Page 4, section 0069]. Kuroi does not teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claim **2,19,36** Kuroi teaches the semiconductor device [Figures 1,2; 101] of claim 4 (or claim 21 or 37) further comprising:

the source [6] having a second edge [Fig. 1, the complement line of line A2 being located above line A1] and the drain having a second edge [same as source];

the gate [5] having a second portion [same as s/d] (for claim 19 extending past {see FIG. 1}); and

a second deep trench structure [AR2, 9, Fig. 1, the complement line of line A2 being located above line A1] located under the second portion of the gate [5] and proximate to the second edge [as above] of the source [6] and the second edge [as above] of the drain [6].

Regarding claims **3,20** Kuroi teaches the semiconductor device of claim 2 (or claim 19) wherein the first edge of the source and drain are approximately parallel to the second edge of the source and drain, and wherein the first and second deep trench structures are approximately parallel to the first and second edges, respectively [see FIG. 1].

Regarding claims **5,22** Kuroi teaches the semiconductor device of claim 4 (or claim 21) wherein the first deep trench structure exhibits a geometry selected from the group consisting of a straight line [See FIG. 1-2, line A2], an angled line, a broken line, and a combination thereof.

Regarding claims **6,23,38** Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 4 (or claims 21,37) further comprising:

an outside edge [Fig. 1, intersection of a 'complement line to line B2' and the line A2] on the source [6];

an outside edge [Fig. 1, intersection of line B2 and line A2] on the drain [6]; and

the first deep trench structure [AR2, 9; adjacent to line A2] having a length extending at least from the outside edge of the source [6] to the outside edge of

the drain [6] [Fig. 1, from line B2-A2 to the source side's 'complement line B2'-A2].

Regarding claims **7,24,39** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 4 (or claims 21,37) wherein the first deep trench structure [AR2, 9; adjacent to line A2] is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof." [Page 5, paragraph 0070, "Thus the trench 2 is filled with silicon oxide films 9A and 9B ... The silicon oxide film 9 is a so-called trench isolation."]. [Page 6, paragraph 0088, "Further, instead of the silicon oxide film 9Ba, for example, a silicon oxynitride film, a PSG film, a BPSG film, an FSG film or the like may be used."]

Regarding claims **8,25,40** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 4 (or claims 21,37) wherein the substrate [1] is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof." [Page 4, paragraph 0067, " As shown in FIGS. 1 to 7, the semiconductor device 101 comprises a semiconductor substrate formed of, e. g., P-type silicon crystal 1."]

Regarding claims **14,31,46** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 4 (or claims 21,37) wherein the gate [5] includes a gate electrode [5A, 5B] and a gate dielectric [4]." [Page 5, paragraph 0072; "a

gate insulating film 4 extends on the main surface 1S of the substrate 1 across the substantial center of the active region AR1 (see FIG. 1). The gate insulating film 4 is formed of a silicon oxide film ..."]. [Page 5, paragraph 0073; " A polysilicon film 5A having a film thickness of about 40nm to 70 nm and a tungsten silicide film 5B having a film thickness of about 50 nm to 100 nm are layered on the gate insulating film 4 ...].

Regarding claims **15,32,47** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 14 (or claims 21,37) wherein the gate electrode [5A, 5B] is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof ". [Page 5, paragraph 0073].

Regarding claims **16,33,48** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 14 (or claims 31,46) wherein the gate dielectric [4] is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof." [Page 5, paragraph 0072].

Regarding claim **17,34,49** Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 4 (or claims 21,37) wherein the first deep trench structure [2,9, line A2] extends around the entire device." [Fig. 1, region AR2].

9. Claims **4,13,21,30,37,45** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shima et al. (US Pat. Pub. 2003/0155592) in further in view of Chen et al. (2003/0006476).

Regarding claim **4**, Shima teaches a semiconductor device [FIG. 10, 11H, 12] comprising;

a substrate [FIG. 11H, "SUBSTRATE"] including a source [31SN] and drain [31DN], the source [31SN] having a first edge [FIG. 12, the horizontal line (marked by 31B) from source to drain passing under the gate] and the drain [31DN] having a first edge [the same line as the source's line] a gate [37N] between the source and drain, the gate having a first portion [FIG. 12, the horizontal line (marked by 31B) from source to drain passing under the gate]; and

a first deep trench structure [FIG. 10, 11H, 12; 32] located directly [see FIG. 12] under the first portion [as above] of the gate viewed in a direction from the gate to the substrate [see FIG. 12], and proximate to the first edge [as above] of the source [31SN] and the first edge of the drain [31DN], wherein the first deep trench structure [32] is of unspecified depth. Shima does not specifically teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claim **21**, Shima teaches a semiconductor device [FIG. 10, 11H, 12] comprising:

a substrate [FIG. 11H, "SUBSTRATE "] including a source [31SN] and drain [31DN], the source having a first edge [as above] and the drain having a first edge [as above];

a gate electrode [37N] on the substrate and between the source [31SN] and drain [31DN], a first portion of the gate electrode [37N] extending past the first edge [as above] of the source and the first edge [as above] of the drain; and

a first deep trench structure [FIG. 10, 11H, 12; 32] located directly under [see FIG. 12] the first portion [as above] of the gate electrode [37N] viewed in a direction from the gate electrode to the substrate and proximate to the first edge [as above] of the source and the first edge [as above] of the drain, wherein the first deep trench structure [32] is of unspecified depth. Shima does not teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claim **37**, Shima teaches a semiconductor device [FIG. 10, 11H, 12] comprising:

a substrate [FIG. 11H, "SUBSTRATE "] having a source [31SN] and drain [31DN], having widths that are substantially equal [see FIG. 10, 12] and each

having a first edge [as above] substantially located along a common line [see FIG. 12, nfet] on the substrate;

a gate electrode [37N] on the substrate and between the source and the drain, the gate electrode having a first portion [as above] extending past the first edge [see FIG. 12] of the source and the first edge of the drain; and

a first deep trench structure [FIG. 10, 11H, 12; 32] located directly under the first portion [as above] of the gate electrode viewed in a direction from the gate electrode to the substrate [see FIG. 12], the first deep trench structure [32] parallel to the common line [as above] on the substrate and proximate to the first edge [as above] of the source and the first edge [as above] of the drain, wherein the first deep trench structure [32] is of unspecified depth. Shima does not teach trench structures deeper than 0.5um. Chen does teach trench structures deeper than 0.5um [page 2, section 0017]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use trenches deeper than 0.5u for the purpose of reducing "an increase in current leakage or a decrease in breakdown voltage" [Page 2, section 0024].

Regarding claims **13, 30, 45** Shima teaches the semiconductor device of claim 4 (or 21, 37) further comprising; a body contact feature adjacent to the source [FIG. 10, 38P, 38N, page 4 section 0073].

Regarding claims **9, 26, 41** Shima teaches the semiconductor device of claim 4 (or 21, 37) wherein the device includes a strained MOS structure [FIG. 10-11A, element 34] [Page 1, 0017-0018; Page4 section 0077].

Allowable Subject Matter

10. Claims **10-12, 27-29, 42-44, 54** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please see the references listed on the PTO-892 form for these pertinent art: Iwamatsu (US Pat. 6495898) and Min (US Pat. Pub. 2003/0211663).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEROME JACKSON
PRIMARY EXAMINER